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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,206	10/09/2003	Mototsugu Fuji	HITA.0441	8330

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EXAMINER	
JACOB, MARY C	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,206	FUJI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 have been presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 23, line 6; page 28, lines 3 and 22; page 31, line 4 refer to elements 0029-0032, however, it may have been intended to reference elements 0028-0031 in Figures 10, 12, 13. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities. The specification appears to be a direct translation from a Japanese document and contains numerous grammatical errors, for example: Abstract, line 3, "wired in direct between"; page 2, line 3, "may be varies"; page 2, line 15, "separates into the portion to realize the

logic"; page 4, lines 3-7, "direction control signal of two way signal". Applicant's assistance is requested in correcting the grammatical errors throughout the specification.

4. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Objections

5. Claims 1-7 are objected to because of the following informalities. Appropriate correction is required.

6. Claims 1-7 have numerous grammatical errors such as the following: Claim 2, line 18-19, "and logic signal is performed"; Claim 3, lines 3-4, "a direction control signal of two-way signal controlled". Applicant's assistance is requested in correcting the grammatical errors.

7. Claim 5, "the priority" should read "a priority".

8. Claim 6, recites, "a means for automatically detecting signal direction of two-way signal between said FPGA module and the device mounting the bridge circuit" that is a repeat of a limitation in claim 4.

9. Claim 7, line 6, "ot", should read, "to".

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

13. The term "a couple" in claims 1 and 4 is a relative term which renders the claim indefinite. The term "a couple" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

14. Claim 2 recites the limitations "the FPGA module", "the verification process", "said logic emulator", "the logic simulation", "the cutting end", "the verification logic", "said logic simulator". There is insufficient antecedent basis for these limitations in the claim.

15. Claim 3 recites the limitation "the logic mounted". There is insufficient antecedent basis for this limitation in the claim.

16. Claim 4 recites the limitation "the device mounting the bridge circuit" and "the program data". There is insufficient antecedent basis for these limitations in the claim.

17. Claim 6 recites the limitation "said two signal directions". There is insufficient antecedent basis for this limitation in the claim.

18. Due to the number of 35 U.S.C. 112, second paragraph rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejection(s), however, the list of rejections may not be inclusive. Applicant should refer to these rejections as examples of deficiencies and should make all necessary corrections to eliminate the 35 U.S.C. 112, second paragraph problems and place the claims in proper format.

Due to the vagueness and a lack of a clear definition of the terminology and phrases used in the specification and claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 102

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

20. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Fuji et al (US Patent 6,564,367).

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a

showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

21. As to Claim 1, Fuji et al teach: a logic verification system utilizing the same FPGA module and the same configuration data in a couple of verification processes of logic emulation and logic simulation (column 1, lines 33-40; column 4, lines 18-42).

22. As to Claim 2, Fuji et al teach: a logic verification system comprising: a logic simulation accelerator including: a device operating on a general purpose processor (Figure 1, element 101; column 4, line 27); a device including a programmable logic device using FPGAs (column 4, lines 21-22); and a bridge circuit for transmitting and receiving data between said device operating on said general purpose processor and said device including the programmable logic device using said FPGAs (Figure 3, switches; column 6, lines 54-56; column 8, lines 16-18), wherein when the FPGA module used in the verification process in said logic emulator and the bridge circuit are wired in direct for all pins of said FPGA module (Figure 3) and the logic simulation is accelerated, the cutting end of the verification logic is assigned to an external interface connector of the FPGA module and the correspondence between each pin of the external interface connector of said FPGA module and logic signal is performed on said logic simulator on said general purpose processor (column 4, lines 30-42; column 5, lines 10-45).

23. As to Claim 3, Fuji et al teach: wherein the logic mounted on said FPGA module is provided with a means for transmitting a direction control signal of two-way signal

controlled therewith to the bridge circuit using an interface (column 17, lines 54-65; column 18, lines 52-61).

24. As to Claim 4, Fiji et al teach: wherein a means for automatically detecting a signal direction of two-way signal between said FPGA module and the device mounting the bridge circuit is provided (column 13, lines 43-45), and the program data of the same FPGA group mounting the verification object logic is used in a couple of verification processes of the acceleration of logic simulation and logic emulation (column 5, lines 10-45).

25. As to Claim 5, Fiji et al teach: wherein said means for automatically detecting the signal direction of two-way signal between said devices is capable of setting a drivability level of output circuits of both devices and giving the priority in determination of signal direction to the device having higher drivability (column 5, lines 35-45).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

27. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji et al as applied to claim 4 above, and further in view of Osaka et al (US Patent 6,496,886).

28. As to Claims 6 and 7, Fuji et al teaches: a means for automatically detecting signal direction of two-way signal between said FPGA module and the device mounting the bridge circuit (column 13, lines 43-45); wherein said means for automatically detecting the signal direction of two-way signal between said devices is capable of setting a drivability level of output circuits of both devices and giving the priority in determination of signal direction to the device having higher drivability (column 5, lines 35-45).

29. Fuji et al does not expressly teach and a means for inputting signal direction of two-way signal to the logic simulator on the general purpose processor, wherein the signal direction of logic simulator and disagreement of signal direction in the FPGA module is detected by comparing said two signal directions.

30. Osaka et al teaches technology to increase transmission speed of a data transfer bus in which a plurality of elements are connected to one transmission line (column 1, lines 6-13). Osaka et al teaches a directional coupling bus system including a bus connected to a plurality of modules each including an interface circuit to transfer digital

data and a printed wiring board connected to the modules (column 2, lines 24-27), and means for inputting signal direction of two-way signal to the logic simulator on the general purpose processor, wherein the signal direction of logic simulator and disagreement of signal direction in the FPGA module is detected by comparing said two signal directions (column 3, lines 12-29; column 10, lines 30-63; column 12, line 54-line 8; column 13, lines 16-27).

31. Fuji et al and Osaka et al are analogous art since they are both directed to the wiring of interconnect between a plurality of logic modules for the purpose of reducing timing delays.

32. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the a means for automatically detecting signal direction of two-way signal between said FPGA module and the device mounting the bridge circuit as taught by Fuji et al to include the means for inputting signal direction of two-way signal to the logic simulator on the general purpose processor, wherein the signal direction of logic simulator and disagreement of signal direction in the FPGA module is detected by comparing said two signal directions as taught by Osaka et al since Osaka et al teaches technology to increase transmission speed of a data transfer bus in which a plurality of elements are connected to one transmission line (column 1, lines 6-13).

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

34. Sample et al (US Patent 6,842,729) teaches generating a hardware prototype of an integrated circuit, the prototype is electrically reconfigurable and may be modified to represent an indefinite number of designs and may be plugged directly into a larger system.

35. Sample et al (US Patent 6,732,068) teaches a hardware emulation system is disclosed which time-multiplexes multiple design signals onto physical logic chip pins and printed circuit board, the reconfigurable logic system comprising a plurality of reprogrammable logic devices, and a plurality of reprogrammable interconnect devices.

36. Quayle et al (US Patent 6,694,464) and Sample et al (US Patent 6,377,912) teach a hardware emulation system comprising a plurality of reprogrammable logic devices, and a plurality of reprogrammable interconnect devices, and a logic analyzer.

37. Evans et al (US Patent 6,279,146) teaches a verification engine for verifying the design of a target system having a plurality of components interconnected by a plurality of target system buses, and switchable communicative circuitry that connects each hardware model input/output pin to a bus line and has a control block controlling the switchable communicative circuitry.

38. Takahashi et al ("110-GB/s Simultaneous Bidirectional Transceiver Logic Synchronized With a System Clock", IEEE Journal of Solid-State Circuits, Vol, 34, No. 11, November 1999) teaches a high-bandwidth CMOS ASIC that features simultaneous bidirectional transceiver logic.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
AU2123

MCJ
7/7/06

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